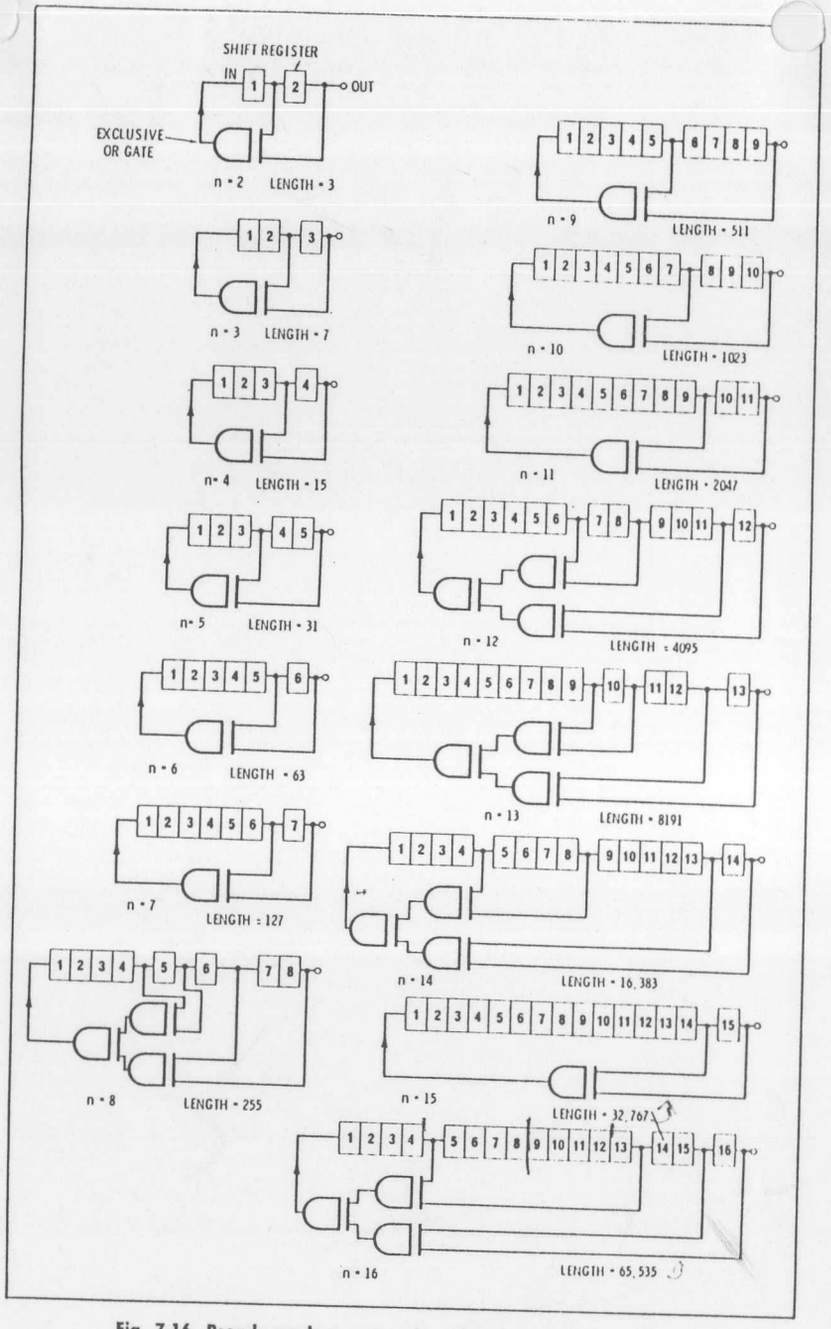

Fig. 7-16. Pseudo-random connections for 2 through 16 stages.

Table 7-2. Register Connections for Longer Sequen

Stages	Sequence Length	Feed EXCLUSIVE OR Gate From Outputs
17	131,071	14 and 17
18	262,143	11 and 18
20	1,048,575	17 and 20
21	2,097,151	19 and 21
22	4,194,303	21 and 22
23	8,388,607	18 and 23
24	16,766,977	19 and 24
25	33,554,431	22 and 25
26	67,074,001	21 and 26
27	133,693,177	19 and 27
28	268,435,455	25 and 28
29	536,870,911	27 and 29
30	1,073,215,489	23 and 30
31	2,147,483,647	28 and 31

7-17A, the noise is integrated with a time constant less than $\frac{1}{20}$ the clock frequency. The same noise pattern repeats every n − 1 clock cycles. If n is made large enough, the noise response becomes essentially dc to the cutoff frequency of the integrator, producing white noise. Filtering converts it into pink noise. A dc blocking capacitor is recommended to keep the integrator centered. Each sequence has an

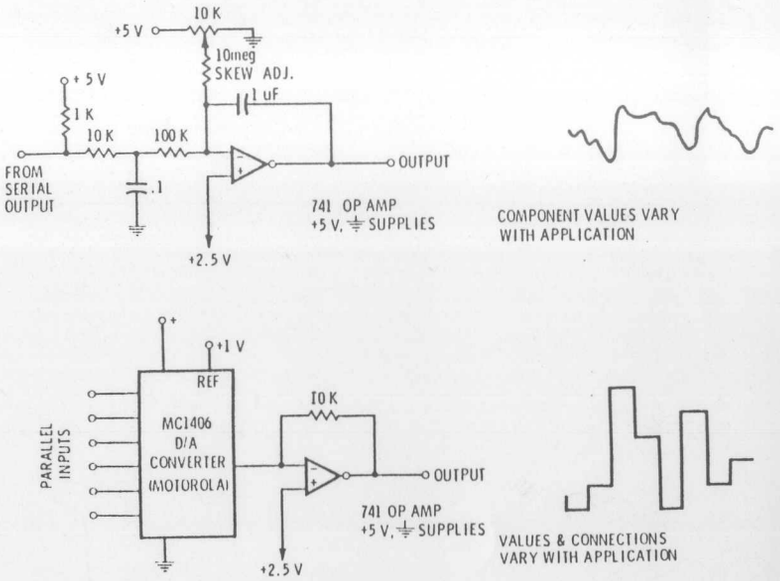

Fig. 7-17. Two ways of converting digital pseudo-random sequences to analog levels or noise.